`timescale 1ns / 1ps

module sipo\_shift\_register\_design(input clk,b,output[3:0]q);

d\_ff dut1(.clk(clk),.d(b),.q(q[3]),.rst());

d\_ff dut2(.clk(clk),.d(q[3]),.q(q[2]),.rst());

d\_ff dut3(.clk(clk),.d(q[2]),.q(q[1]),.rst());

d\_ff dut4(.clk(clk),.d(q[1]),.q(q[0]),.rst());

endmodule

// d flip flop

module d\_ff (

input clk,

input d,

input rst,

output reg q);

always @(posedge clk)

begin

if (rst)

q <= 1'b0;

else

q <= d;

end

endmodule